

U.S. UTILITY Patent Application					
<b>KU</b> O.I.P.C. SCANNED O.A. Am				PATENT DATE	
APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/768246	D F	457	180	2811	PARKE/KI Thomas
<b>APPLICANTS</b> Kazuishi Higashi Norihiro Tsukahira Takahiro Yonezawa Yoshihiko Yagi					
<b>TITLE</b> Method of forming a built-in board of a printed circuit board					
PTO-2040 12/69					
ISSUING CLASSIFICATION					
<b>ORIGINAL</b> CLASS      SUBCLASS		<b>CROSS REFERENCE(S)</b> <b>SUBCLASS (ONE SUBCLASS PER BLOCK)</b>			
<b>INTERNATIONAL CLASSIFICATION</b>					
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket					
<b>TERMINAL DISCLAIMER</b>		<b>DRAWINGS</b> Sheets Drwg.      Figs. Drwg.      Print Fig.		<b>CLAIMS ALLOWED</b> Total Claims      Print Claim for O.G.	
<input type="checkbox"/> The term of this patent, subsequent to (date), has been disclaimed.		(Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. ( )		(Primary Examiner) (Date)		<b>ISSUE FEE</b>	
<input type="checkbox"/> The terminal ( ) months of this patent have been disclaimed.		(Legal Instruments Examiner) (Date)		Amount Due      Date Paid	
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